Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A**
2. **B**
3. **C**
4. **D**
5. **E**
6. **F**
7. **N/C**
8. **GND**
9. **Y**
10. **G**
11. **H**
12. **N/C**
13. **N/C**
14. **VCC**

**.042”**

**13 12 11 10**

**14**

**1**

**2**

**L**

**S**

**3**

**0**

**MASK**

**REF**

**9**

**8**

**7**

**.038”**

**3 4 5 6**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: LS30**

**APPROVED BY: DK DIE SIZE .038” X .042” DATE: 4/29/16**

**MFG: TEXAS INSTRUMENTS THICKNESS .012” P/N: 54LS30**

**DG 10.1.2**

#### Rev B, 7/1